PATENT

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Himanshu S. Amin

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant:	Khoi Phan, *et al.*	Examiner:	Erick J. Rekstad
Serial No:	09/553,841	Art Unit:	2163
Filing Date:	April 21, 2000		

Title: SYSTEM AND METHOD FOR VISUALLY MONITORING A SEMICONDUCTOR PROCESSING SYSTEM

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Applicants submit this brief in triplicate in connection with an appeal of the above-identified patent application. Please charge $330.00 for the fee associated with this brief to Deposit Account No. 50-1063[AMD468US].

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I. Real Party in Interest (37 C.F.R. §1.192(c)(1))

The real party in interest in the present appeal is Advanced Micro Devices, Inc., the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. §1.192(c)(2))

Appellants, appellants' legal representatives, and/or the assignee of the present application are not aware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. §1.192(c)(3))

Claims 1-23 are pending in the subject application. The rejection of claims 1-23 is appealed.

IV. Status of Amendments (37 C.F.R. §1.192(c)(4))

No claim amendments have been entered subsequent the Final Office Action.

V. Summary of Invention (37 C.F.R. §1.192(c)(5))

The subject invention generally relates to visually monitoring an interior portion of a processing (*e.g.*, develop) chamber in a semiconductor processing system. (Abstract). In particular, one or more image collectors are integrated into a develop chamber to collect images of the interior of the develop chamber and generate an image signal indicative of a visual representation thereof. (p.12, ll.25-32). This image signal is conveyed to and received by a viewing station, which displays the visual representation to an operator of the semiconductor processing system. (p.12, l.32 – p.13, l.1). The foregoing improves visual inspection of the develop process by mitigating any need use a step ladder to visually inspect the process from the top of the system, which conventionally can exceed ten feet in height. (p.12, ll.2–13).

VI. Statement of the Issues (37 C.F.R. §1.192(c)(6))

A. Whether claims 1-3, 5, 7, 10-12, 15-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sanada (US 5,843,527) in view of Choi, *et al.* (US 6,089,763).

B. Whether claims 4, 6, 8-9 and 13-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sanada (US 5,843,527) in view of Choi, *et al.* (US 6,089,763) and in further view of Stern, *et al.* (US 6,603,874).

VII. Grouping of Claims (37 C.F.R. §1.192(c)(7))

For the purposes of this appeal only, the claims are grouped as follows:

Claims 1-23 stand or fall together.

VIII. Argument (37 C.F.R. §1.192(c)(8))

A. Rejection of Claims 1-3, 5, 7, 10-12, 15-23 Under 35 U.S.C. §103(a)

Claims 1-3, 5, 7, 10-12, and 15-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sanada (US 5,843,527) in view of Choi, *et al.* (US 6,089,763). It is respectfully requested that this rejection be withdrawn for at least the following reason. Sanada and Choi, *et al.*, alone and in combination, do not teach or suggest ***all*** the claim limitations.

i. *Applicable law*

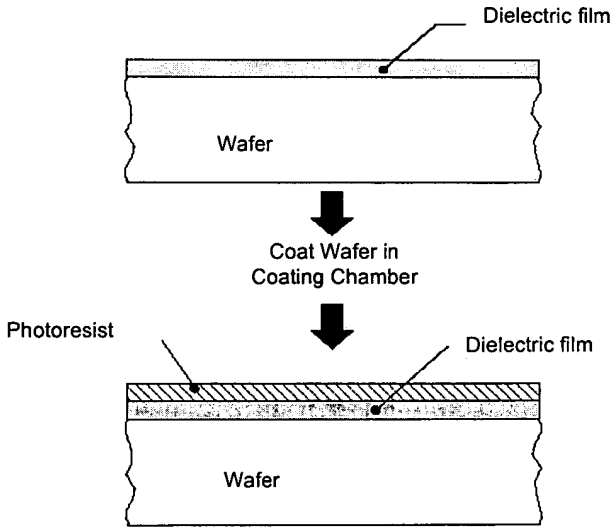
> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

ii. ***The combination of Sanada and Choi, et al. does not teach or suggest all the claim limitations; thus, Sanada in view of Choi, et al. does not make obvious the subject claims.***

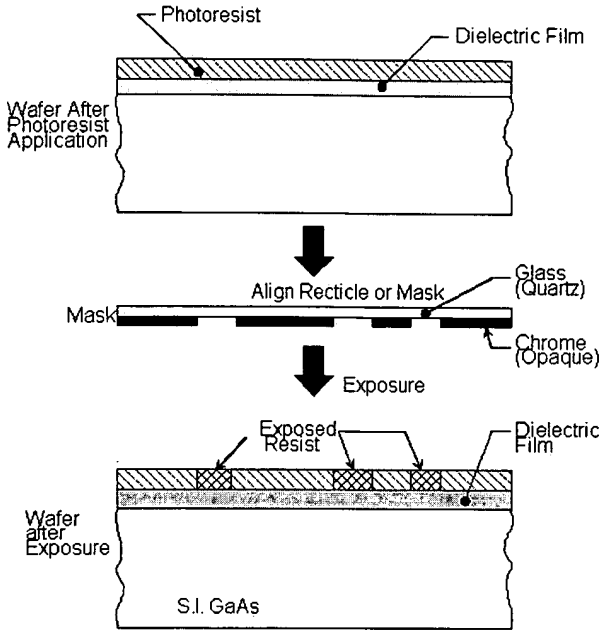
Independent claims 1, 15 and 19 recite a visual monitoring system that employs an ***image collector*** to capture reflected energy from inside a ***develop chamber*** and transmit a signal indicative of the interior of the ***develop chamber***. The combination of Sanada and Choi, *et al.* does not teach or suggest employing an image collector in connection with a develop chamber to

generate a signal indicative of the interior of the develop chamber as recited in the subject claims. Instead, Sanada and Choi, *et al.* disclose monitoring a ***coating*** (and not a develop) process.

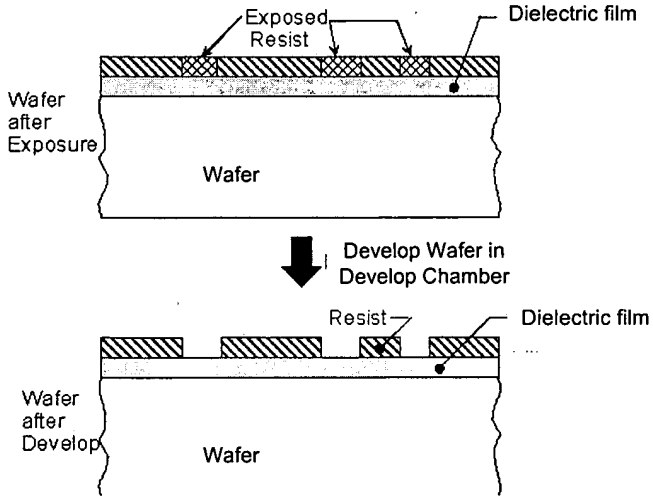
As known, conventional semiconductor processing systems commonly include two side-by-side lines of processing tools, which respectively comprise various processing modules. Typically, one side includes prime, coat and soft bake modules, while the other side includes post etch bake (PEB), develop and hard-bake modules. In general, a robotic mechanism automatically transfers wafers from one module to another module during semiconductor fabrication such that a plurality of wafers can be concurrently fabricated. For example, the robotic mechanism can place a wafer in a coating module where a photoresist is applied to the wafer. This step is depicted in the following diagram.



Upon coating the wafer, it can be moved from the coating module to a soft bake module where the wafer is heated to remove, *via* evaporation, solvents. Then, the wafer can be moved from the soft bake module to a cooling module to reduce its temperature. From the cooling module, the wafer can be conveyed to another module(s) where a mask is aligned and the wafer is exposed. Mask alignment and wafer exposure are illustrated in the following diagram.



After exposure, the wafer can be conveyed to a devlop chamber for development, as shown in the following diagram. From the devlop chamber, the wafer can be transferred to various other modules for hard banking, inspection, etching, photoresist removal, *etc.*



Typically, while one wafer (or set of wafers) moves from a first module to another module, a different wafer (or set of wafers) is transitioned to the first module such that several wafers (or sets of wafers) can be concurrently processed at different stages of fabrication. Thus, a wafer (or set of wafers) can be coated by the coating chamber, while a different wafer (or set of

wafers) is developed in the develop chamber. (*See* Peter Van Zant, *Microchip Fabrication: A Practical Guide to Semiconductor Processing* (4th ed. 2000); ITT GaAsTEK and Virginia Tech., http://www.mse.vt.edu/faculty/hendricks/mse4206/GaAsTEK/Lithography/ladv.htm (2004)). Hence, the coating chamber and the develop chamber are disparate chambers, utilized at disparate stages in semiconductor fabrication, for disparate steps in the fabrication process.

The Examiner asserts the specification of the subject application at page 4, line 24 states "a chamber is for ***both*** coating, developing, heating, etc." (*See* Advisory Action, p.2) (Emphasis added). Applicants' representative respectfully submits the Examiner is reading terms into applicants' specification. The term "both" is not recited at page 4, line 24. Rather, this section of the subject application notes that a chamber can be one of several disparate processing units. Specifically, page 4, line 24 recites "[i]n the track system, the chamber 120 is a processing unit, such as a coater, developer, heating unit, cooling unit, etc." However, this section does not state the chamber is "both" a coater and developer as alleged by the Examiner. Moreover, the ***claimed invention recites*** an aspect of the invention wherein the chamber is simply a ***develop chamber***. As noted *supra*, both Sanada and Choi, *et al.* disclose monitoring ***coating chambers***, not develop chambers.

Furthermore, the Examiner concedes "Sanada does not teach the system being a develop chamber" (*See* Final Office Action, p.3, §2), but asserts that since Choi, *et al.* discloses a spin unit that can be a spin coater or spin developer, "it would be obvious to one skilled in the art at the time of the invention to use the imaging system of Sanada with the spin developer of Choi, *et al.* because the coater and developer are both considered spin units." (*See* Final Office Action, p.3, §2). It is respectfully submitted that a mere assertion that the coater and developer of Choi, *et al.* are simply spin units does not make applicants' claimed invention obvious. Rather, "[a] teaching or suggestion to make the claimed combination and a reasonable expectation of success must both be found in the prior art...." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As discussed in detail below, neither Sanada nor Choi, *et al.* provide a teaching or suggestion to be combined or modified in view of the other to render the subject claims obvious.

In particular, Sanada, as conceded by the Examiner, discloses a ***coating*** solution applying method and apparatus and is silent regarding a develop chamber. Since Sanada is only directed at semiconductor ***coating***, it is readily apparent that Sanada does not provide any teaching,

suggestion, motivation or desirability to be modified to include visual monitoring of a develop chamber (which is non-existent in Sanada) as recited in the subject claims. Choi, *et al.* discloses both a coater and developer and utilization of a CCD camera; however, Choi, *et al.* teaches ***visual monitoring of the coater*** with the CCD camera to control the supply of a ***coating*** solvent (*See* col.8, ll.41-67) and does not contemplate monitoring its develop chamber. Since Choi, *et al.* discloses a monitoring system but does not contemplate monitoring its disclosed develop chamber, it is readily apparent that it would not be obvious at the time of the invention to utilize any monitoring system to monitor the develop chamber, let alone the monitoring system taught by Sanada. Thus, similar to Sanada, Choi, *et al.* does not provide any teaching, suggestion, motivation or desirability to be modified to include visual monitoring of a develop chamber, as recited in the subject claims.

Since Sanada and Choi, *et al.*, individually and in combination, do not teach or suggest ***all*** the claimed limitations or provide any motivation or desirability to be combined or modified in view of each other to teach or suggest ***all*** the claimed limitations, the asserted combination does not make obvious the subject claims and is erroneous. "The teaching or suggestion to make the claimed combination and a reasonable expectation of success must both be found in the prior art, not in applicants' disclosure" (*In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)) and "the mere fact that references can be modified does not render the modification obvious unless the cited art also suggests the desirability of the modification" (*In re Mills,* 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)).

Thus, it appears that 20/20 hindsight is being impermissibly employed with applicants' specification as a roadmap to make the purported combination; the rationale proffered to modify and combine Sanada and Choi, *et al.* is to achieve benefits identified in applicants' specification, which overcome problems associated with conventional systems and/or methods. Applicants' representative respectfully submits that this is an unacceptable and improper basis for a rejection under 35 U.S.C. §103. In essence, this rejection is based on an assertion that it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in applicants' specification. This sort of rationale has been condemned by the Court of Appeals for the Federal Circuit. *See, for example, Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593 (Fed. Cir. 1987).

In view of the above, it is respectfully submitted that this rejection of independent claims 1, 15 and 19 (and claims 2-3, 5, 7 and 10-12, 16-18, and 20-23, which respectively depend therefrom) should be withdrawn.

B. Rejection of Claims 4, 6, 8-9 and 13-14 Under 35 U.S.C. §103(a)

Claims 4, 6, 8-9 and 13-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sanada (US 5,843,527) in view of Choi, *et al.* (US 6,089,763) and in further view of Stern, *et al.* (US 6,603,874). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Claims 4, 6, 8-9 and 13-14 depend from independent claim 1. (*See In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed Cir. 1988) ("If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious."). Thus, for at least the reasons provided *supra*, this rejection should be withdrawn.

IX. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-23 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Respectfully submitted,

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X. Appendix of Claims (37 C.F.R. §1.192(c)(9))

1. A system that visually monitors semiconductor processing, comprising:

a develop chamber; and

an image collector located at least partially within the develop chamber, the image collector collects energy reflected from inside the develop chamber and transmits a signal indicative of interior of the chamber.

2. The system of claim 1 further includes a light source that illuminates the interior of the develop chamber to enable the image collector to obtain a visible image of the interior of the chamber.

3. The system of claim 2, the light source is a light emitting diode.

4. The system of claim 2, the light source is a fiber optic cable with a light emitting portion located within the develop chamber.

5. The system of claim 2, further comprises a coater chamber that provides photoresist material on a substrate, the light source provides light at a wavelength so as not to expose the photoresist material.

6. The system of claim 2, the develop chamber develops photoresist material on a substrate, the light source provides light at a wavelength so as not to expose the photoresist material.

7. The system of claim 2, the image collector includes a camera module that collects the images and provides an electrical signal indicative of a visual representation of the interior of the chamber.

8. The system of claim 7, the camera module is connected with one end of a fiber optic cable, a lens being connected with another end of the fiber optic cable for collecting the images from the interior of the chamber and providing the image signal to the camera module, the camera module converting the image signal into the electrical signal.

9. The system of claim 8, the lens is faceted to receive reflected light from a plurality of discrete directions within the chamber so that the image signal is formed of an image from each of the discrete directions.

10. The system of claim 7 further includes a viewing station that receives the electrical signal and displays a visual representation of the interior of the chamber according to the electrical signal.

11. The system of claim 10, the viewing station includes a controller that selectively controls activation of the camera module.

12. The system of claim 11, the controller further controls the light source.

13. The system of claim 1, the image collector includes a fiber optic cable having a light receiving end disposed within the chamber for collecting images of the interior of the chamber, another end of the fiber optic cable being connected to a camera module that provides the image signal indicative of the interior of the chamber, the camera module converting the image signal into an electrical signal indicative of the interior of the chamber.

14. The system of claim 13, the light receiving end of the fiber optic camera includes a lens for receiving light from a plurality of discrete directions within the chamber so that the image signal is formed of an image from each of the discrete directions.

15. A system that visually monitors an internal part of a semiconductor processing system, comprising:

imaging means for collecting images of an interior of an enclosed developer and providing an image signal indicative of a visual representation of the interior of the developer; and

viewing means for receiving the image signal and providing a visual representation of the interior of the chamber.

16. The system of claim 15, the imaging means includes a camera having a lens portion located within the chamber to collect the images and provide the image signal.

17. The system of claim 15 further includes illumination means for illuminating the interior of the chamber to facilitate collecting images of the interior of the chamber by the camera.

18. The system of claim 17 further includes means for selectively controlling at least one of the camera and the illumination means.

19. A method for visually monitoring an interior of an enclosed developing chamber in a semiconductor processing system, comprising the steps of:

collecting visual images of the interior of the chamber and providing an image signal indicative thereof; and

displaying a visual representation of the interior of the enclosed chamber based on the image signal.

20. The method of claim 19 further includes the step of illuminating the interior of the enclosed chamber to facilitate collecting of visual images.

21. The method of claim 20, the step of illuminating includes emitting light within the chamber at a wavelength which does not interfere with processing within the chamber.

22. The method of claim 19 further includes the step of controlling the steps of emitting and collecting so that the visual representation includes images of processing within the chamber.

23. The method of claim 19, visual representation is displayed remotely from the semiconductor processing system.